PATENT

Attorney Docket No. FULCP009

ASYNCHRONOUS SYSTEM-ON-A-CHIP INTERCONNECT

RELATED APPLICATION DATA

The present application claims priority from U.S. Provisional Patent Application No. 60/444,820 for ASYNCHRONOUS INTERCONNECT SYSTEM filed on February 3, 2003 (Attorney Docket No. FULCP009P), the entire disclosure of which is incorporated herein by reference. The present application also claims priority from U.S. Patent Application No. 10/136,025 for ASYNCHRONOUS CROSSBAR CIRCUIT WITH DETERMINISTIC OR ARBITRATED CONTROL filed on April 30, 2002 (Attorney Docket No. FULCP001), and U.S. Patent Application No. 10/212,574 for TECHNIQUES FOR FACILITATING CONVERSION BETWEEN ASYNCHRONOUS AND SYNCHRONOUS DOMAINS filed on August 1, 2002 (Attorney Docket No. FULCP002), the entire disclosures of both of which are incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

The present invention relates to asynchronous digital circuit design and in particular to asynchronous circuitry for interconnecting a variety of system resources in the context of a system-on-a-chip.

A so called "system-on-a-chip" (SOC) is typically designed with a number of modules, each of which has its own clock. For example, such a system might include a memory controller, an I/O interface (e.g., PCI or HyperTransport), internal peripherals (e.g., SRAM or computing logic), computing resources (e.g., one or more CPUs), and some kind of interconnect for allowing the modules to interact with each other. In a typical SOC, the